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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,757	10/19/2001	Nghia Tran		4411

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,757	TRAN ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35-51* is/are allowed.

6)☒ Claim(s) *52,54,55,57-62 and 64-75* is/are rejected.

7)☒ Claim(s) *53,56 and 63* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *04 March 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 52, 54-55, 57-62, and 64-75 are rejected under 35 U.S.C. 102(e) as being anticipated by Pierce et al. (US 5,581,199).

Pierce discloses, in fig. 16, a programmable input/output device (inherent CMOS device see US 4,870,302 col. 2, lines 50+ as disclosed in col. 1, lines25+) as capable of operating at multiple logic standards (broadly interpreted as different modes; see col. 18, line 48 - col. 19, line 65) comprising:

an input/output terminal (PAD A or B);

a plurality of programmable elements (PIPs; col. 18, lines 57+);

an input buffer (174) having circuitry (175-183) controlled by at least one of the plurality of programmable elements to select between a first logic standard (asynchronous) and a second logic standard (synchronous, col. 19, lines 14-31) wherein the second logic standard is a differential logic standard (Q and QL in 181 or AIN1 and AIN2 since they are both two different signals);

an output buffer (173) having circuitry (161-172) controlled by at least one of the plurality of programmable elements (PIPs) to select between the first logic standard and the second logic standard;

wherein at least one programmable element is coupled (indirectly) to the input buffer and at least one programmable element (194) is coupled to the output buffer; and

wherein the input buffer and the output buffer are controlled by the same programmable element (PIPs before 165 that controls tristate; see col. 18, lines 64+).

Response to Arguments

Applicant's arguments filed 1/31/2003 have been fully considered but they are not deemed to be persuasive.

Applicant argues, on page 21 of the Amendment filed 1/31/2003, that "nowhere in Pierce are I/O circuits shown that can switch between multiple logic standards as described in applicants' claims." However, Pierce teaches an input buffer (174) having circuitry (175-183) controlled by at least one of the plurality of programmable elements to select between a first logic standard (asynchronous) and a second logic standard (synchronous, col. 19, lines 14-31) wherein the second logic standard is a differential logic standard (Q and QL in 181 or AIN1 and AIN2 since they are both two different signals). Examiner has broadly interpreted the asynchronous signal as a first logic standard and the synchronous signal as a second logic standard. Also, Examiner has broadly interpreted the synchronous signals Q and QL of 181 as a differential logic standard since the register 181 outputs two different synchronous logic signals. It is noted that "the PTO applies to the verbiage of the proposed claims the broadest reasonable

meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art," *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

Allowable Subject Matter

Claims 35-51 are allowed.

Claims 53, 56, and 63 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Pierce, taken alone or in combination of other references, does not teach or fairly suggest a programmable input/output device capable of operating at multiple logic standards comprising, among other things, an input buffer comparing the received input signals to the reference signal to produce a differential signal, as set forth in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Daniel D. Chang
Primary Examiner
Art Unit 2819

DC
March 24, 2003

DANIEL CHANG
PRIMARY EXAMINER